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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/512,149 02/23/2000		Vishnu K Agarwal	MI22-1322	3457	
21567	7590 . 11/16/2004		EXAMINER		
WELLS ST.		n	PIZARRO CRESPO, MARCOS D		
SPOKANE, V	ΓAVENUE, SUITE 1300 WA 99201		ART UNIT	PAPER NUMBER	
 ,			2814		

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

· · · · · · · · · · · · · · · · · · ·		Application	on No.	Applicant(s)			
Office Action Summary		09/512,14		AGARWAL, VISHI	NU K		
		Examiner		Art Unit			
		Marcos D.	Pizarro-Crespo	2814			
Period for	The MAILING DATE of this communica		<u> </u>	orrespondence add	dress		
A SHOF THE MA - Extensic after SIX - If the pe - If NO pe - Failure t Any repl	RTENED STATUTORY PERIOD FOR ALLING DATE OF THIS COMMUNICATION of time may be available under the provisions of 3 (6) MONTHS from the mailing date of this communication for reply specified above is less than thirty (30) directly of reply is specified above, the maximum statute or reply within the set or extended period for reply will, y received by the Office later than three months after patent term adjustment. See 37 CFR 1.704(b).	ATION. 7 CFR 1.136(a). In no ever cation. ays, a reply within the state by period will apply and wi by statute, cause the apple	ent, however, may a reply be tim story minimum of thirty (30) days Il expire SIX (6) MONTHS from ication to become ABANDONEI	nely filed s will be considered timely the mailing date of this co D (35 U.S.C. § 133).			
Status							
1)⊠ R	Responsive to communication(s) filed on 21 October 2004.						
2a)∐ Ti	his action is FINAL . 2b)	⊠ This action is n	on-final.				
-	Since this application is in condition for allowance except for formal matters, prosecution as to the ments is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.						
Disposition	n of Claims						
4a 5)⊠ C 6)⊠ C 7)⊠ C	 4) Claim(s) 1.4-14.56-70 and 72-108 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) Claim(s) 1.4-14.56-70.72-77.79-82.90-98 and 104 is/are allowed. 6) Claim(s) 78.83.86-89.99-103 and 105-108 is/are rejected. 7) Claim(s) 84 and 85 is/are objected to. 8) Claim(s) are subject to restriction and/or election requirement. 						
Application	n Papers						
9)∐ Th	e specification is objected to by the E	xaminer.					
10)□ Th	e drawing(s) filed on is/are: a	on is/are: a)☐ accepted or b)☐ objected to by the Examiner.					
Aj	Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
	Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority und	der 35 U.S.C. § 119						
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 							
Attachment(s)) of References Cited (PTO-892)		4) Interview Summary	(PTO-413)			
2) Notice of 3) Information	f Draftsperson's Patent Drawing Review (PTO- tion Disclosure Statement(s) (PTO-1449 or PTO o(s)/Mail Date <u>43</u> .		Paper No(s)/Mail Da)-152)		

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Attorney's Docket Number: MI22-1322

Filing Date: 2/23/2000

Claimed Foreign Priority Date: none

Applicant(s): Agarwal

Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the amendment in paper no. 41 filed on 10/21/2004.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after the final rejection in paper no. 39, mailed on 5/21/2004. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/21/2004 has been entered.

Acknowledgment

2. The amendment in paper no. 41, filed on 10/21/2004, responding to the Office action in paper no. 39, mailed on 10/21/2004, has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 1, 4-14, 56-70, and 72-108.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

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4. Claims 78 and 105 are rejected under 35 U.S.C 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time

the application was filed, had possession of the claimed invention.

5. Claim 78 describes a first electrode layer comprising a monolithic unitary material. The description in the original disclosure fails to support this limitation in the claim. The specification (see, e.g., pp.7/II.4-7) listed several materials from which to make the first electrode layer. A *monolithic unitary material*, however, is not one of

them.

6. Claim 105 describes a layer within a layer. Specifically, the claim recites a dielectric material layer formed within the high-K dielectric layer. The description in the original disclosure fails to support this limitation in the claim. The specification describes a high-K capacitor dielectric region 20 comprising dielectric material layer 22 and dielectric material layer 24 (see, e.g., pp.7/II.10-16, and figs. 1 and 2), but it fails to describe any of the dielectric material layers 22, 24 as formed within another high-K dielectric layer.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

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8. Claims 83, 86-89, 99, 101, 102, and 105 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schuele (US 5760474) in view of Ramakrishnan (US 5192871).

- 9. Regarding claim 83, Schuele (see, *e.g.*, fig. 6) shows most aspects of the instant invention including an integrated circuitry comprising:
 - > A substrate 30
 - > An insulative material **37** formed over the substrate **30**
 - > An opening formed in the insulative material 37
 - > A capacitor **75** comprising:
 - A first electrode layer **50** formed within the opening
 - A dielectric region 60 formed over the first electrode layer 50 and within the opening
 - A second electrode layer 70 formed over the dielectric region 60

Schuele, however, fails to show that the dielectric region is formed of a high-K material comprising a crystalline portion and an amorphous portion. Ramakrishnan, on the other hand, teaches that it would be highly advantageous for Schuele's dielectric region to comprise a high-K dielectric material having a crystalline portion and an amorphous portion. This structure would provide the sought-after high-dielectric constant that characterizes crystalline dielectric materials, and at the same time would prevent the migration of foreign materials that may adversely affect the dielectric constant of the capacitor dielectric layer. See, e.g., Ramakrishnan, col.1/II.45-50, col.32/II.35-37, and col.3/II.23-30.

It would have been obvious at the time of the invention to one of ordinary skill in the art to have a high-K dielectric material having a crystalline portion and an amorphous portion for the capacitor dielectric region of Schuele, as suggested by Ramakrishnan, to protect the dielectric properties of the layer.

- 10. Regarding claim 86, Ramakrishnan (see, *e.g.*, col.2/II.50-52) shows the portion of the amorphous material comprising at least 70% amorphous phase.
- 11. Regarding claim 87, Ramakrishnan shows that the high-K dielectric layer may comprise Ta_2O_5 (see, e.g., col.3/II.53).
- 12. Regarding claim 88, Ramakrishnan (see, *e.g.*, col.2/II.50-52) shows the portion of the amorphous material comprising greater than 90% amorphous phase.
- 13. Regarding claim 89, Ramakrishnan shows that the portions of amorphous and crystalline materials may be from different materials (see, e.g., col.2/ll.48).
- 14. Regarding claim 99, Ramakrishnan teaches that the amorphous material is provided in an amount effective to reduce leakage current through the crystalline material (see, e.g., col.2/II.68-col.3/II.3).
- 15. Regarding claims 101 and 102, Schuele shows that the capacitor comprising a portion of a DRAM circuitry.
- 16. Regarding claim 105, Ramakrishnan shows the dielectric material region comprising a high-K dielectric layer (see, *e.g.*, col.3/II.53).
- 17. Claim 100 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schuele/Ramakrishnan in view of Wu (US 5998247).

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18. Regarding claim 100, Schuele/Ramakrishnan shows most aspects of the instant invention (see, e.g., paragraph 9 above with respect to claim 83). They also teach that a DRAM includes a capacitor **75** (see, e.g., Schuele/fig. 6). However, they fail show the capacitor also comprising a portion of a logic circuitry. Wu (see, e.g., col.1/ll.12-15), on the other hand, teaches that logic circuits with DRAM devices are demanded as high-performance devices that reduce power consumption and increase packing density.

It would have been obvious at the time of the invention to one of ordinary skill in the art to include the capacitor of Schuele/Ramakrishnan into a logic circuit, as suggested by Wu, to reduce power consumption.

- 19. Claims 103 and 106-108 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schuele/Ramakrishnan in view of Venkatraman (US 6093966), Chen (US 6100137) and Yu (US 6274443).
- 20. Regarding claims 103 and 106-108, Schuele/Ramakrishnan shows most aspect of the instant invention (see, e.g., paragraph 9 above with respect to claim 83). They, however, fail to show the outermost portion of the insulating material comprising an antireflective coating layer made of SiON. Venkatraman (see, e.g., col.4/II.54-59), on the other hand, teaches that providing Schuele/Ramakrishnan's outermost portion of the insulating material with an antireflective layer would minimize the reflections from underlying features during the definition of the opening so that a uniform distribution of the critical dimensions of the opening is obtained. Yu (see, e.g., col.5/II.2-3, col.15/II.44-47) teaches that one of the most commonly used ARC is SiON, which enhances the imaging effect in photolithographic processing. Chen (see, e.g., col.2/II.15-25) further

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teaches that a SiON layer would provide the outermost portion of the insulating material of Schuele/Ramakrishnan with an improved antireflective coating.

It would have been obvious at the time of the invention to one of ordinary skill in the art to provide Schuele/Ramakrishnan's outermost portion of the insulating material with a SiON antireflective layer, as suggested by Venkatraman/Yu/Chen, so that a uniform distribution of the critical dimensions of the opening is obtained.

Allowable Subject Matter

- 21. Claims 1, 4-14, 56-70, 72-77, 79-82, 90-98, and 104 are allowed.
- 22. Claims 84 and 85 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

23. The applicants argue:

The examiner states that the specification lists several materials from which to make a first electrode layer and that a monolithic unitary material is not one of them. The examiner is confusing the phrase "monolithic unitary" as being a description for a composition, when in fact is directed to a structure configuration, that is, a material that is structured as a monolithic unitary material. Such a monolithic unitary structure is clearly shown as element 136 of figure 9 of the original application. Therefore, the written description for claim 78 is satisfied and the 112, first paragraph, rejection is improper.

The examiner responds:

The applicants have failed to provide a clear, concise, and meaningful definition that is supported in the specification as originally filed to the term "monolithic unitary material". Broadly arguing that the term refers to element **136** as shown in figure 9 does not satisfy the written description requirement of 112, first paragraph, of using full, clear, concise, and exact terms. It is not evident from figure 9, and its accompanying written description in the specification, that element **136** is a monolithic unitary material. From

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the original disclosure, it follows that element **136** is a capacitor storage node (see, *e.g.*, pp.13/II.3) and also the materials from which it may be made (see, *e.g.*, pp.7/II.4-7). The original disclosure, however, fails to describe element **136** as a monolithic unitary material.

24. The applicants argue:

To modify the Schuele's dielectric layer **60** using Ramakrishnan's teachings, as suggested by the examiner, to have an amorphous portion for the purpose of preventing the including of foreign materials in the high-K dielectric layer **60**, that is, using the amorphous portion as a diffusion barrier, is redundant. Schuele already provides extensive teachings to a barrier layer in the Schuele capacitor (see, e.g., col.3/II.1-15,40-60; col.4/II.54-67; col.5/II.40-55, abstract, and background). The examiner suggests modifying Schuele to include what Schuele has already provided. Logically, one skilled in the art would not look to Ramakrishnan to modify Schuele to have what Schuele has already provided.

The examiner responds:

Schuele uses a barrier layer to prevent diffusion from the plug to the capacitor lower electrode and from the lower electrode to the dielectric layer (see, e.g., col.3/II.56-62). Ramakrishnan, on the other hand, uses the amorphous portion of a dielectric layer inter alia to prevent the inclusion of foreign materials from layers located above the dielectric layers, e.g., from the top electrode to the capacitor dielectric region.

Conclusion

25. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is (703) 872-9306. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

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- 26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marcos D. Pizarro-Crespo at (571) 272-1716 and between the hours of 9:30 AM to 8:30 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (571) 272-1705.
- 27. Any inquiry of a general nature or relating to the status of this application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

28. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/310, 438/240, 361/313/	11/10/2004
Other Documentation:	
Electronic Database(s): EAST (USPAT, EPØ, JPO)	11/10/2004

Marcos D. Pizarro-Crespo
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Art Unit 2814

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PRIMARY PRIMARY

MDP/mdp 3/4/2003